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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/749,668	12/30/2003	Theodore S. Moise IV	TI-36398	9759

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EXAMINER	
KALAM, ABUL	

ART UNIT	PAPER NUMBER
2814	

NOTIFICATION DATE	DELIVERY MODE
11/25/2008	ELECTRONIC

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Notice of the Office communication was sent electronically on above-indicated "Notification Date" to the following e-mail address(es):

uspto@ti.com

Office Action Summary	Application No.	Applicant(s)	
	10/749,668	MOISE ET AL.	
	Examiner	Art Unit	
	Abul Kalam	2814	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *08 September 2008*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-5,21 and 22* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-5,21 and 22* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

Continued Examination Under 37 CFR 1.114

A request for continued examination under 37 CFR 1.114, including the fee set forth in 37 CFR 1.17(e), was filed in this application after final rejection. Since this application is eligible for continued examination under 37 CFR 1.114, and the fee set forth in 37 CFR 1.17(e) has been timely paid, the finality of the previous Office action has been withdrawn pursuant to 37 CFR 1.114. Applicant's submission filed on August 6, 2008, has been entered.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

1. **Claims 1-5, 21 and 22** are rejected under 35 U.S.C. 103(a) as being unpatentable over **Moise et al. (US 6,211,035**; previously cited, hereinafter, Moise**)** in view of **Fox et al. (6,627,930**; previously cited, hereinafter, Fox**)**.

With respect to **claim 1, Moise** teaches an integrated circuit comprising:

An array of ferroelectric memory cells **(Figs. 6a-6f; col. 2: lns. 13-16)**, each cell **(col. 8: lns. 64-67)** having a capacitor stack **(624, Fig. 6c)** having an upper electrode **(610, Fig. 6a)**, a lower electrode **(606, Fig. 6a)**, a lower conductive barrier layer **(604, Fig. 6a)** underlying the lower electrode **(606)** and a single ferroelectric core layer **(608, Fig. 6a)** disposed between the upper and lower electrodes, wherein the integrated

circuit further comprises a conductive contact **(320, Fig. 6c)** formed under at least one of the capacitor stacks **(624)**, wherein the conductive contact **(320)** has a cross section at a contact portion that contacts a bottom portion of the capacitor stack **(624)**, that is about as large as that of the ferroelectric cores **(Fig. 6c; col. 9: lns. 1-67, col. 10: lns. 1-13)**.

Thus, **Moise** teaches all the limitations of the claim with the exception of disclosing: wherein the single ferroelectric core layer has a crystallization in the (001) family and at least 40% of the domains of the single ferroelectric core layer are functionally oriented with respect to the capacitor stack.

However, **Fox** teaches a capacitor stack **(10_2; FIG. 1B)** having a single ferroelectric core layer **(18)** with a crystallization in the (001) family **(FIG. 1B; col. 4: lns. 1-21)**, wherein at least about 40% of the domains are functionally oriented with respect to the capacitor stack.

Regarding the claimed "at least about 40% of the domains are functionally oriented with respect to the capacitor stack," **Fox** discloses that the entire single ferroelectric core layer **(18; FIG. 1B)** has a crystallographic texture of <001>, and thus it is implicit that about 50-100% of the domains are functionally oriented with respect to the capacitor stack **(see FIG. 1B; col. 4: lns. 9-11, 17-19)**.

Furthermore, note that the specification contains no disclosure of either the *critical nature of the claimed*, "at least 40% of the domains are functionally oriented with respect to the capacitor stack," or any unexpected results arising therefrom. Where patentability is said to based upon particular chosen dimension or upon another variable

recited in a claim, the Applicant must show that the chosen dimension are critical. *In re Woodruff*, 919 F.2d 1575, 1578, 16 USPQ2d 1934, 1936 (Fed. Cir. 1990).

Therefore, it would have been obvious to one of ordinary skill in the art at the time of the invention to incorporate the teaching of **Fox** into the device of **Moise**, to form the ferroelectric core layer having a crystallographic texture of <001>, because such crystallization structures are generally preferred due to the orientation of the polarization **(col. 4: lns. 17-21)**.

With respect to **claim 2, Moise and Fox** teach the all the limitations of the claim, as set forth above in claim 1, with the exception of disclosing: wherein about 45 to about 75% of the domains are functionally oriented with respect to the capacitor stack.

However, it would have been obvious to one of ordinary skill in the art to form a ferroelectric layer with about 45 to about 75% of the domains functionally oriented, as claimed, because **Fox** teaches ferroelectric layers in which the direction of the polarization magnitude is generally from the bottom electrode toward the top electrode **(col. 4: lns. 9-11)**. Furthermore, note that absent evidence of disclosure of criticality for the range or dimensions giving unexpected results, it is not inventive to discover optimal or workable ranges or dimensions by routine experimentation. See *In re Aller*, 220 F.2d 454, 105 USPQ 233, 234 (CCPA 1955).

With respect to **claim 3, Moise and Fox** teach the integrated circuit of claim 1 above. Furthermore, **Moise** teaches wherein the ferroelectric core layer comprises a PZT core **(608, Fig. 6a)**.

Regarding the limitation of "a PZT core having a switched polarization of at least about 60 $\mu C/cm^2$," the specification contains no disclosure of either the *critical nature of the claimed*, "switched polarization of at least about 60 $\mu C/cm^2$," or any unexpected results arising therefrom. Where patentability is said to base upon particular chosen dimension or upon another variable recited in a claim, the Applicant must show that the chosen dimension is critical. *In re Woodruff*, 919 F.2d 1575, 1578, 16 USPQ2d 1934, 1936 (Fed. Cir. 1990).

With respect to **claim 4, Moise and Fox** teach the integrated circuit of claim 1 above. Furthermore, **Moise** teaches a dielectric layer **(1050, Fig. 10c)** covering the array of memory cells **(1024, Fig. 10b)**, the dielectric layer **(1050)** having a conductive contact **(1060, Fig. 10d)** over each ferroelectric core **(608, Fig. 6a)**, the conductive contacts each having a cross section about as large as that of the ferroelectric core layer **(Figs. 6a and 10d)**.

With respect to **claim 5, Moise and Fox** teach the integrated circuit of claim 1 above. Furthermore, **Moise** teaches wherein the electrodes **(606, 610; Fig. 6a)** are adjacent opposing sides of the ferroelectric cores **(608, Fig. 6a).**

Regarding the limitation, "electrodes adjacent opposing sides of the ferroelectric cores have a collective thickness of at least about 200 nm thick," the specification contains no disclosure of either the *critical nature of the claimed*, "collective thickness of at least about 200 nm," or any unexpected results arising therefrom. Where patentability is said to base upon particular chosen dimension or upon another variable

recited in a claim, the Applicant must show that the chosen dimension is critical. *In re Woodruff*, 919 F.2d 1575, 1578, 16 USPQ2d 1934, 1936 (Fed. Cir. 1990).

With respect to **claim 21, Moise and Fox** teach the integrated circuit of claim 1 above. Furthermore, **Moise** teaches a dielectric layer **(1070, Fig. 10d)** covering the array of memory cells, the dielectric layer having an additional conductive contact **(1080, Fig. 10d)** over each ferroelectric core layer **(608; Figs. 6a-6c)**, the additional conductive contacts **(1080)** having a cross section about as larger or larger than that of the ferroelectric core layer **(1024)** and extending through said dielectric layer **(1070)** to a metal interconnect layer **(1062) (Figs. 6a and 10d)**.

With respect to **claim 22**, as best interpreted by the Office**, Moise** teaches an integrated circuit comprising:

An array of ferroelectric memory cells **(Figs. 6a-6f; col. 2: lns. 13-16)**, each cell **(col. 8: lns. 64-67)** having a capacitor stack **(624, Fig. 6c)** comprising:

a lower conductive barrier layer **(604, Fig. 6a)**;

a lower electrode **(606)** over the barrier layer **(604)**;

a single ferroelectric core layer **(608)** disposed above the lower electrode;

an upper electrode **(610)** over the single ferroelectric core layer **(608)**;

an upper barrier **(614)** over the upper electrode **(610)**;

wherein the integrated circuit further comprises a first conductive contact **(1060, Fig. 10d)** formed over the capacitor stack, and a second conductive contact **(1020, Fig. 10d)** formed under the capacitor stack, and wherein the first and second conductive

contacts **(1060 and 1020)** each have a cross section at a contact portion of the capacitor stack **(Fig. 10d)**, that is about as large as that of the ferroelectric core layer **(Figs. 6c and 10d; col. 9: lns. 1-67, col. 10: lns. 1-13)**.

Thus, **Moise** teaches all the limitations of the claim with the exception of disclosing: wherein the single ferroelectric core layer has a crystallization in the (001) family and at least 40% of the domains of the single ferroelectric core layer are functionally oriented with respect to the capacitor stack.

However, **Fox** teaches a capacitor stack **(10_2; FIG. 1B)** having a single ferroelectric core layer **(18)** with a crystallization in the (001) family **(FIG. 1B; col. 4: lns. 1-21)**, wherein at least about 40% of the domains are functionally oriented with respect to the capacitor stack.

Regarding the claimed "at least about 40% of the domains are functionally oriented with respect to the capacitor stack," **Fox** discloses that the entire single ferroelectric core layer **(18; FIG. 1B)** has a crystallographic texture of <001>, and thus it is implicit that about 50-100% of the domains are functionally oriented with respect to the capacitor stack **(see FIG. 1B; col. 4: lns. 9-11, 17-19)**.

Furthermore, note that the specification contains no disclosure of either the *critical nature of the claimed*, "at least 40% of the domains are functionally oriented with respect to the capacitor stack," or any unexpected results arising therefrom. Where patentability is said to based upon particular chosen dimension or upon another variable recited in a claim, the Applicant must show that the chosen dimension are critical. *In re Woodruff*, 919 F.2d 1575, 1578, 16 USPQ2d 1934, 1936 (Fed. Cir. 1990).

Therefore, it would have been obvious to one of ordinary skill in the art at the time of the invention to incorporate the teaching of **Fox** into the device of **Moise**, to form the ferroelectric core layer having a crystallographic texture of <001>, because such crystallization structures are generally preferred due to the orientation of the polarization **(col. 4: lns. 17-21)**.

Response to Arguments

2. Applicant's arguments filed August 6, 2008, have been considered but are not persuasive.

With respect to the claims 1 and 22, and the Moise et al. reference (US 6,211,035), Applicant argues that lower contact plugs 320 of fig. 6c and 1020 of Fig. 10b of Moise appear to be clearly smaller than that of the ferroelectric capacitor cores of PZT layer 608. The argument is not persuasive because the claim recites "wherein the conductive contact has a cross section...that is about as large or larger than that of the ferroelectric core layer," and figs. 6c and 10b of Moise clearly show that the conductive contact (320 in fig. 6c and 1020 in fig. 10b) has a cross section that is about as large as that ferroelectric core layer (608 in fig. 6a, which has been patterned in fig. 6c). Note that the cross section of the conductive contact does not have to be as large or larger than that of the ferroelectric core layer; the cross section of the conductive contact only has to be about as large as that of the ferroelectric layer.

With respect to the Fox et al. reference (US 6,627,930), Applicant argues that Fox does not teach a single ferroelectric core layer. The argument is not persuasive, because Fox clearly discloses a single ferroelectric core layer 18 in Fig. 1B, a single ferroelectric core layer 22 in Fig. 2B, a single ferroelectric core layer 32 in Fig. 3B, and single ferroelectric core layer 42 in Fig. 4B, all of which have a crystallization in the (001) family, wherein at least 40% of the domains of the layer are functionally oriented with respect to the capacitor stack (col. 4, lns. 17-19). Furthermore, note that claim 1 recites "an integrated circuit, comprising," and thus, claim 1 is inclusive and not exclusive. Thus, Applicant's argument that that Fox teaches away from a single ferroelectric layer by disclosing multiple ferroelectric layer structures, is not persuasive because although the limitation requires a single ferroelectric layer in the (001) family, the limitation does not exclude the use of other ferroelectric layers in the capacitor structure. Also note, the primary reference of Moise also discloses a single ferroelectric core layer, and that the Fox reference is a secondary reference, whose teaching is incorporated into the primary references, not the other way around as argued by the Applicant ("such a modification would render the structure of Fox et al. unsatisfactory for it's intended purpose," pg. 8 of the Remarks). Finally, regarding the motivation to combine Fox with Moise, Fox teaches that although it is more difficult to grow, ferroelectric layers having a <001> crystallographic texture are generally preferred due to the orientation of the polarization (col. 4, lns. 17-20).

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Abul Kalam whose telephone number is (571)272-8346. The examiner can normally be reached on Monday - Friday, 9 AM - 5 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Wael M. Fahmy can be reached on 571-272-1705. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/A. K./
Examiner, Art Unit 2814

/Phat X. Cao/
Primary Examiner, Art Unit 2814